UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/580,619 | 05/24/2006 | Raymond J.E. Hueting | GB03 0213 US1 | 5566 |

65913 7590 02/19/2009

NXP, B.V.
NXP INTELLECTUAL PROPERTY DEPARTMENT
M/S41-SJ
1109 MCKAY DRIVE
SAN JOSE, CA 95131

| EXAMINER | |
|---|---|
| RAO, SHRINIVAS H | |
| ART UNIT | PAPER NUMBER |
| 2814 | |

| NOTIFICATION DATE | DELIVERY MODE |
|---|---|
| 02/19/2009 | ELECTRONIC |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/580,619 | HUETING ET AL. | |
| | Examiner | Art Unit | |
| | STEVEN H. RAO | 2814 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *12 December 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1 and 3-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1,3-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## *Response to Amendment*

Applicants' amendment filed on December 08, 2008 has been entered and forwarded to the Examiner on December 12, 2008.

Therefore Claims 1,3 and 8 as amended by the amendment and claims 11-14 presently newly added and claims 3-7 and 9-10 as previously recited are currently pending in the Application.

Claim 2 has been cancelled.

## *Information Disclosure Statement*

To date no Ids has been filed in this case.

## *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 to 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Fujishima. (U.S. patent No. 5,981,996 herein after Fujishima) ( also submitted by Applicants' in their IDS). ( for response to Applicants' contentions see section below).

*With respect to claim 1Fujishima describes an* insulated gate field effect transistor, comprising:
a source region of first conductivity type ( fig.l, 104) ;a body region of a second conductivity type opposite to the first conductivity type adjacent to the source region ( fig.1,111) ; a drift region of exclusively the first conductivity type adjacent to the body region ( fig.1,102) ; a drain region of the first conductivity type adjacent to the drift region, ( fig l, 109) so that body and drift regions are arranged between the source and drain regions ( fig.l), the drain region being of higher doping density than the drift region ( col. 10 line 10 and inherent because drain region below drift and therefore higher doping density) ; and insulated trenches extending from the source region through the body region and into the drift region each trench having sidewalls and including an

insulator on the sidewalls ( figs.l,4 105, insulator-406), and a conductive gate electrode between the insulating sidewall, (fig. 1,107) wherein the base of each trench is filled with an insulator plug adjacent to substantially all of the length of the drift region between the body region and drain region .( to the extent understood- fig. 1, 112) and the respective gate electrode is provided in the trench over the plug adjacent to the source and body ( fig.1 107).

*With respect to claim 3 Fujishima describes an* insulated gate field effect transistor according to claim 1 wherein the doping concentration in the body region is in the range of about 0.5x1017 cm3 to about 3 x 10 17 $cm^{-3'}$ and the doping concentration in the drift region) is in the range about 1 x 1015 cm-3 to about 2x I 017 $cm^{"3}$ . (col. 8 lines 45,46-49,54; col. 9-55 ;10-5,10). *With respect to claim 4 Fujishima describes an* insulated gate field effect transistor according to claim 1 wherein the plug is of dielectric filler filling the trench between the insulator on the sidewalls adjacent to the drain region. ( Fig. 1,106 ).

*With respect to claim 5 Fujishima describes an* insulated gate field effect transistor according to claim 1 having a semiconductor body (fig.l, 111) having opposed first-(fig. 1 ) second major surfaces (fig. 1), wherein the source region (104) is at the first major surface over the region, the body region (111)is over the drift region (102) and the drift region (102)is over the drain region (109), and the trench (105)extends from the first major surface towards the second major surface through the source (104), body (111) and drift (102) regions.

*With respect to claim 6 Fujishima describes an* insulated gate field effect transistor according to claim 5 having a plurality of cells each cell having a source region at centre of the cell surrounded by the insulated trench. (col. 12 line 61 ).

*With respect to claim 7 Fujishima describes an* insulated gate field effect transistor according to claim 6 wherein the cells have a hexagonal geometry. (well known in the art e.g. Hark also cited by applicants in their IDS).

*With respect to claim 8 Fujishima describes an* insulated gate field effect transistor according to claim 6 wherein the trench (figs. 105 ) has gate oxide (Fig.106) on the sidewalls, and the trench adjacent to the drift region is filled with filler oxide between the gate oxide (fig. 112) on the sidewalls on either side of the trench. ( fig.112 ).

*With respect to claim 9 Fujishima describes an* insulated gate field effect transistor according to claim 5 having a plurality of cells ( col. 12 line 61 ) arranged as stripes across the first major surface (Fig.1) with alternating trenches (105) and source regions (104).

With respect to claim10 Fujishima describes an insulated gate field effect transistor according to claim 6 wherein the cell pitch is in the range of about 0.2 microns to about 0.7 microns. ( col. 9 lines 35 to col. 10 lines 19).

With respect to claims 11 and 12 Fujishima describes an insulated gate field effect transistor according to claims 1 /11 wherein the doping concentration in the drift region is non-uniform.( it is inherent that the portion of the drift region in figs., e.g. fig.1 at a higher level "i.e. adjacent drift region have lower doping concentration than the portion of the drift region at a lower level ( adjacent to the drain region 109, see also response to applicants arguments section below ).

With respect to claim 13 Fujishima describes an insulated gate field effect transistor according to claim 12 wherein the non-uniform doping concentration in the drift region is linearly graded from the higher doping concentration adjacent to the drain region to the lower doping concentration adjacent to the base region. .( it is inherent that the portion of the drift region in figs., e.g. fig.1 at a higher level "i.e. adjacent drift region have higher doping concentration than the portion of the drift region at a lower level will have lower concentration i.e. linearly graded adjacent to the drain region 109, see also response to applicants arguments section below ).

With respect to claim 14 An insulated gate field effect transistor according to claim 11 wherein the doping concentration in the body region is in the range of about 0.5x 1017 cm-3 to about 3x 10~7 cm-3, and the doping concentration in the drift region is in the range of about lxl0~5 cm-3 to about 2x10~7 cm-3. (rejected for reasons under claim 3 above - col. 8 lines 45,46-49,54; col. 9-55 ;10-5,10 and response to arguments section below.).

## *Response to Arguments*

1. Applicant's arguments filed on 12/08/2008 have been fully considered but they are not persuasive for the following reasons :

2. Applicants' first contention that Drawings shows a plug, because the Specification states a plug may be a dielectric is noted.

3. It is further noted that one of ordinary skill in the art identifies a plug with a conductive body ( as also stated in various dictionaries e.g. IEEE, etc.) and a dielectric

filler is NOT conductive . While an Applicant can be his own lexicographer, Applicants' definition of terms should not be Where applicant acts as his or her own lexicographer to specifically define a term of a claim contrary to its ordinary meaning, *Process Control Corp. v. HydReclaim Corp.*, 190 F.3d 1350, 1357, 52 USPQ2d 1029, 1033 (Fed. Cir. 1999). The term plug in claims 1, 3-14 is used by the claim to mean dielectric filler , while the accepted meaning is conductive body ."

Applicants' argument with respect to claim1, that the applied Fujishima reference does not disclose/teach " the drift region of exclusively of the first conductivity type adjacent to the body region" is not persuasive as Applicants' arguments are not commensurate in scope with the presently recited claims.

Applicants' claim1 presently recites :

"1. (currently amended) An insulated gate field effect transistor, comprising:
a source region of first-a first conductivity type;
a body region of second a second conductivity type opposite to the first conductivity type adjacent to the source region;
a drift region of exclusively the first conductivity type adjacent to the body region;
a drain region of f the first conductivity type adjacent to the drift region, so that body and drift regions are arranged between the source and drain regions, the drain region being of higher doping density than the drift region; and "

Therefore presently the claims only require that a drift region be exclusively the first conductivity type and physically located near or adjacent to the body region.

The applied Fujishima reference shows in figure1 ( reproduced below) a drift region 102 as stated in the rejection).

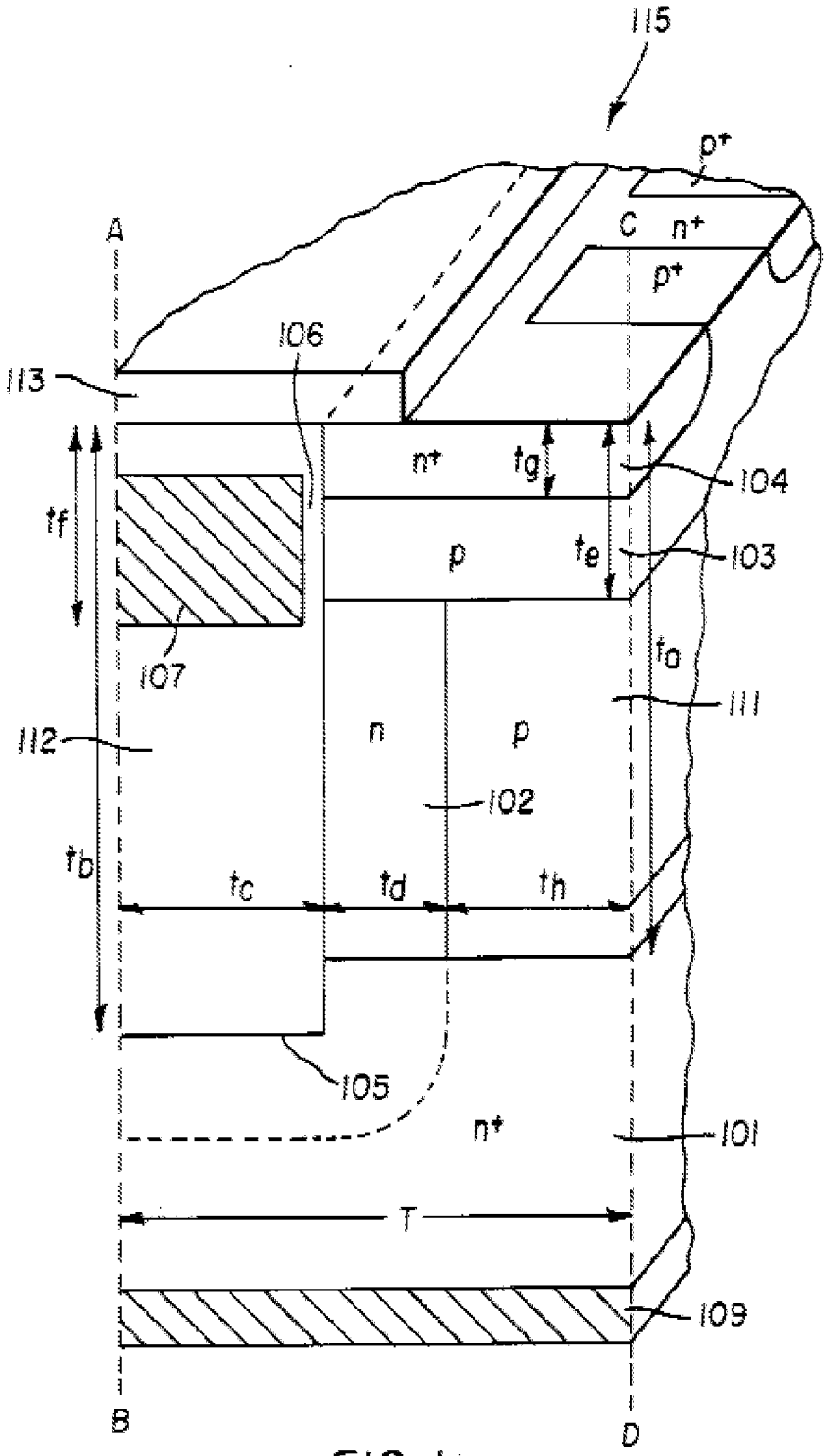
115
p+
A
C
n+
p+
106
113
n+
tg
104
tf
p
te
103
107
ta
111
112
n
p
102
tb
tc
td
th
105
n+
101
T
109
B
D

FIG. 1

As seen above and described at least in Fujishima's specification page col. 8 lines 41-44 , drift region 102 is exclusively of the first conductivity type namely n-type and physically located near or adjacent to the body region.( similar to Applicants' adjacent to body region 2 ( fig.1) near ( adjacent) drift region 10).

Applicants' are arguing Fujishima's impurity layer 111 which is p-type should now be included in drift region 102 to form a device having drift regions ( 102, and 111) includes multiple conductivity types.

However, this is contrary to Fujishima's disclosure which only identified drift region as element 102 which is exclusively n-type.

Applicants' have not provided any reason why region 111 ( not identified as drift region by Fujishima ) should be included as the drift region.

Therefore Applicants' conclusion that the device of Fujishima does not include a drift region with exclusively one conductivity type is not persuasive and contrary to the plain teachings of Fujishima.

If Applicants' desire to maintain this argument they may add language similar to below in the claims, to provide arguments commensurate in scope with their arguments.

" Wherein the region between the base region and the substrate is made up exclusively of n-type conductivity."

Therefore presently recited claim1 does not distinguish over applied art and is finally rejected.

Dependent Claims 2-14 were alleged to be allowable because of their dependency upon allegedly allowable claim 1.

However, as seen above claim 1 is not allowable, therefore dependent claims 2 to 14 are also not allowable.

Applicants' argument with regard to claims 11-13 starts with cancelled claim 2 , the applicants; arguments w.r.t to cancelled claim 2 need not be addressed because it is moot as Applicants' have cancelled claim 2.

With regard to claims 11-13 , which are presented for the first time in the amendment it is noted that the standard for providing explanations in the rejections is not that every attorney or application understand it but rather one skilled in the art should understand it.

In the present context it is noted that one skilled in the art would understand that in the doping process ( One can refer to standard text books like Wolf, Ghandi, etc. ) doped regions are characterized by dopant profile, which determines the amount of dopant actually added in the doped region as a function of depth. Further , transistors undergo many thermal excursions during processing which allow dopant diffusion that alter junction depth and concentration wherein the areas at the top of the region have higher concentration than the deeper regions.

Therefore the rejections have provided all necessary result or characteristic to establish inherency .

Applicants argument w.r.t claim 13 ( and 3) that Fujishima does not disclose Fujishima does not support the assertion of inherency because the actual disclosure of Fujishima describes the drain drift region has having a specific surface impurity concentration of $1.1 \times 10^{\sim 7}$ cm -3. Fujishima, col. 8, lines *53-54* is partially correct. But the rejection was based on portions of Fujishima col. 8 lines 45,46-49 and col. 9 line 55 and col. 10 lines 5 and 10 when the complete rejection is considered, Applicants' arguments are not persuasive.

Therefore claims 11 to 13 are also finally rejected.

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to STEVEN H. RAO whose telephone number is (571)272-1718. The examiner can normally be reached on 8.30-5.30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1714. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Steven H Rao/
Examiner, Art Unit 2814

/Howard Weiss/
Primary Examiner, Art Unit 2814